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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): YOR920030259US1 (8728-635)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

Application Number	Filed
10/643,193	8/18/03
First Named Inventor	
Bhavna Agarwal	
Art Unit	**Examiner**
2857	West, J.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record. Registration number 43,584

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Frank V. DeRosa
Typed or printed name

516-692-8888
Telephone number

5/9/07
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: A. Bhavnagarwala et al.

Examiner: West, Jeffrey R.

Serial No.: 10/643,193

Group: Art Unit 2857

Filed: August 18, 2003

Docket: YOR920030289US1 (8728-635)

For: **CIRCUITS AND METHODS FOR CHARACTERIZING RANDOM VARIATIONS IN DEVICE CHARACTERISTICS IN SEMICONDUCTOR INTEGRATED CIRCUITS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Statement in Support of Pre-Appeal Brief Request for Review

This paper is being filed in support of Applicants' Pre-Appeal Brief Request for Review. A Notice of Appeal has been filed herewith in response to the Final Office Action mailed on January 9, 2007. Applicants respectfully contend that the claim rejections set forth in the Final Office Action are clearly erroneous as a matter of fact and/or law.

Claim Rejections – 35 U.S.C. § 101

The Examiner finds that claims 1, 3-13, 15-19, 26, 27, 29 and 32-38 include non statutory subject matters that are directed to the manipulation of abstract ideas which do not accomplish a practical application. Applicants respectfully assert that these findings are the result of an improper legal analysis, and that claims 1, 10, 26 and 27, at the very least, are clearly directed to statutory subject matter. The subject matters of claims 1, 10, 26 and 27 are directed to real world, practical applications for characterizing device mismatch in a semiconductor integrated circuit. For instance, claim 1 recites a method for characterizing device mismatch which includes:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor

devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

In formulating the 101 rejections, the Examiner contends that:

> **in determining whether the claim is for a "practical application", the focus is not on whether the steps taken to achieve a particular result are "useful, tangible and concrete", but rather that the final result is "useful, tangible and concrete". (see p. 17 of Final Action).**

With regard to claim 1, the Examiner finds that:

> **This final step of processing does not produce a useful, concrete and tangible result, but is instead a result of internal data manipulation that is not externally conveyed. Also since the resulting processing is not used for an intended purpose, it appears to be only a starting point for future application. (see p. 5 of the Final Action)**

These findings are *fundamentally* flawed on various grounds. First of all, the Examiner notes that the focus is not the particular steps claimed, yet the Examiner's analysis narrowly focuses on the final step of "processing" to assess utility of claim 1, while ignoring the claimed subject matter as a whole. The Examiner further errs in characterizing the "processing" step as mere "internal data manipulation", despite the more specific language of *processing DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.* Irrespective of whether the claimed "processing" step can be properly characterized as internal data manipulation by a computer, where the processing results are not externally conveyed, this characterization does not support a finding, per se, that the claim is directed to an abstract idea with no practical application. Indeed, all computers generally operate by manipulating and processing binary data, for example. The determinative issue the significance of the data and what process is being performed by the computer.

In this regard, the Examiner has not explained how the processing *processing DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.* Indeed, the very step of *processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices* is *per se* directed to a useful, tangible and concrete result of

obtaining distribution data for device mismatch for the real world practical application of characterizing device mismatch in semiconductor integrated circuits. The record clearly demonstrates that methods for characterizing device mismatch have significant "real world" value and practical application in the technical field of semiconductor circuit design and fabrication.

For example, Applicants' specification explains the usefulness and importance of device mismatch characterization techniques in the field of semiconductor fabrication, for purposes of providing robust circuit designs and enhancing functional yield for a given process, where Applicants describe conventional experimental techniques have been developed for purposes of characterizing device mismatch. For instance, FIG. 1 of Applicants' specification describes a conventional method using a test circuit with an array of transistors to collect measurements of drain current ID vs. gate voltage VG (I-V) characteristics for each transistor in the array and process such I-V measurement data to extract various parameters such a Vt, transconductance, drain currents, etc. and generate distributions for such parameters to characterize device mismatch. Moreover, the Conti reference cited by the Examiner, which teaches a test structure for collecting test data for mismatch characterization of MOS transistors, is further objected evidence in the record of the utility and practical real world applications of device mismatch characterization methods.

Moreover, the Examiner errs in finding that the *resulting processing is not used for an intended purpose, it appears to be only a starting point for future application.* This finding fails to consider that the intended purpose of the claimed subject matter is to "determine a distribution of device mismatch between transistor devices" based on processing the related DC characteristic data. In other words, the Examiner fails to recognize that the claimed subject matter specifically recites a process of obtaining and processing DC voltage data for the intended purpose determining a distribution of device mismatch between the first and second semiconductor transistor devices, which is clearly a useful and tangible real world result.

Therefore, for at least the above reasons, there is no reasonable basis for the Examiner's finding that the subject matter of claim 1 is directed to an abstract idea with no real world result. Further, to the extent that claims 10, 26 and 27 are rejected on similar grounds, the same reasoning give above for claim 1 applied to refute the Examiner's findings of non-utility of claims 10, 26 and 27. The 101 rejections should be withdrawn.

Claim Rejections - 35 U.S.C. §103

Claims 1,10, 26, and 27 (among other claims) stand rejected as being unpatentable over U.S. Patent No. 6,275,094 to Cranford in view of Conti. Other obviousness rejections are asserted using Cranford and Conti as the primary references as applied to claims 1, 10, 26 and 27. For purposes of this request for pre-appeal brief review, Applicant will only address the impropriety of obviousness rejections of claims 1, 10, 26 and 27.

In general, the obviousness rejections are based on clear misinterpretations and mischaracterizations of the teachings of Cranford and Conti as applied to the claimed inventions, as well as a text book example of the use of hindsight reasoning to selectively pick among unrelated, disparate prior art teachings to derive the claimed subject matter with absolutely no motivation for combining the reference teaching.

For example, the Examiner's erroneously contends essentially that Cranford discloses in FIG. 4, Col. 7, lines 7-36 and Col. 8, lines 1-4) the claimed step of *processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices* (Col. 7, lines 20-23, and 28-36), *wherein the DC voltage characteristic data comprises an output DC voltage* V_{OUT} *as a function of an input DC voltage* V_{IN}, *wherein* V_{IN} *is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein* V_{OUT} *is obtained at a common node connection of the first and second semiconductor transistor devices.*

However, Cranford teaches in the cited sections a method for dynamically generating a voltage to correct threshold mismatch between transistor devices in a differential amplifier to thereby correct for manufacturing offset (See Abstract; and Col. 7, lines 20-23). This is done by performing a Fast Fourier Transform analysis of output harmonics to determine mismatch between input and output harmonics where any mismatch is translated into a voltage representative of the offset between the differential transistor pair, and where the feedback voltage is returned to the differential pair to eliminate the effect of offset (see, Col. 4, lines 34-44, and Col. 7, lines 20-42). The input and output signals are sine waves (see FIG. 6, Col. 7, lines 44-47).

In this regard, the Examiner fails to explain how a *process of correcting threshold mismatch by performing a fast Fourier transform analysis to detect harmonic differences identified by the FFT between sinusoidal input-output signals* as taught by Cranford is even remote the same or similar to the claimed process of *processing the DC voltage characteristic*

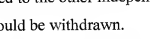
data (which is *output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}) to determine a distribution of device mismatch between the first and second semiconductor transistor devices* as claimed in claims 1 and 26, for example. Indeed, Cranford does not even rely on DC voltage characteristic data but rather differences in harmonics of sinusoidal input-output voltages.

In any event, the Examiner acknowledges that Cranford does not teach that the *the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region* (See page 8 of the Final Office Action). Instead, the Examiner erroneously relies on Conti in this regard, contending that Conti teaches a test structure for threshold voltage misplaced by obtaining DC voltage characteristic data for adjacent transistors. The Examiner concludes essentially that it would be obvious to modify the teachings of Cranford to include the use of DC voltage characteristic data of a transistor pair operating in the subthreshold regime as taught by Conti

The Examiner's reliance on Conti in support of the claim rejections is *grossly* misplaced as *Conti* teaches a mismatch model based on measurements of drain current ID (see page 173, second column on bottom). As such, Conti teaches away from the claimed process of obtaining. *DC voltage characteristic data* (DC Vout as a function of DC Vin) *with first and second semiconductor transistor devices operating in a subthreshold region.*

Moreover, the Examiner takes a quantum leap to explain motivation for modifying Cranford with Conti. Again, Cranford does not teach DC voltage characteristic data. Moreover, Cranford's process of correction of mismatch does not operate with the transistor pairs under consideration being operated in the "subthreshold regime". In fact, Cranford teaches a real-time correction process in which the transistor pairs under consideration are not biased to operate in the subthreshold regime (or the circuit would not work). The Examiner's proposed combination of Conti and Cranford as applied to claim 1 make no sense on technical or legal grounds. The same reasoning applied to the other independent claims 10, 26 and 27. Accordingly, the obviousness rejections should be withdrawn.

Respectfully submitted,



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